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TRANSMITTAL OF APPEAL BRIEF (Large Entity)					Docket No. ITO.0048US	
In Re Applicat	ion Of: Stephen J. Hud	gens				
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Application No	o. Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.	
10/633,873	August 4, 2003	Ahmed N. Sefer	47795	2826	5270	
Invention: P	rocessing Phase Change	Material to Improve Programmi	ng Speed			
COMMISSIONER FOR PATENTS:						
Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed on:						
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Timothy N. Trop	, Reg. No. 28,994					
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(Date)

Signature of Person Mailing Correspondence

Nancy Meshkoff

Typed or Printed Name of Person Mailing Correspondence

cc:



In re Applicant:

Serial No.:

Stephen J. Hudgens

10/633,873

August 4, 2003 Filed:

For: Processing Phase Change Material

to Improve Programming Speed

Art Unit:

2826

Examiner:

Ahmed N. Sefer

Atty Docket: ITO.0048US

(P16245)

Assignee:

**Intel Corporation** 

Mail Stop Appeal Brief-Patents Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

## **APPEAL BRIEF**

Date of Deposit: I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postai Service as first class mail with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

# TABLE OF CONTENTS

REAL PARTY IN INTEREST	3
RELATED APPEALS AND INTERFERENCES	
STATUS OF CLAIMS	
STATUS OF AMENDMENTS	6
SUMMARY OF CLAIMED SUBJECT MATTER	7
GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL	9
ARGUMENT	
CLAIMS APPENDIX	12
EVIDENCE APPENDIX	14
RELATED PROCEEDINGS APPENDIX	15

### REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation.

### RELATED APPEALS AND INTERFERENCES

None.

# **STATUS OF CLAIMS**

Claims 1-10 (Withdrawn).

Claims 11-15 (Canceled).

Claims 16-20 (Rejected).

Claim 21 (Canceled).

Claims 22-25 (Rejected).

Claims 26-30 (Withdrawn).

Claims 16-20 and 22-25 are rejected and claim 23 is the subject of this Appeal Brief.

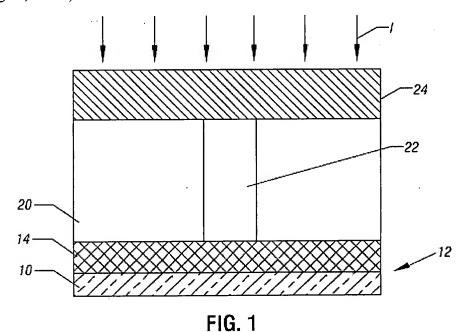
# STATUS OF AMENDMENTS

All amendments have been entered. The Reply to Final Rejection filed on April 16, 2007 contained no amendments.

## SUMMARY OF CLAIMED SUBJECT MATTER

In the following discussion, the independent claims are read on one of many possible embodiments without limiting the claims:

- 16. A semiconductor memory device comprising:
  a semiconductor substrate (Figure 1, 10) (Specification at page 2, lines 18-20);
  and
- a layer of chalcogenide (Figure 1, 24) material over said substrate, said chalcogenide material including a species to reduce the grain size of the chalcogenide material and a species to increase the crystallization speed of said chalcogenide material (Specification at page 3, lines 6-16).
- 22. The device of claim 16 including an insulator (Figure 1, 20) over said substrate and under said chalcogenide material (Specification, page 2, lines 24-25).
- 23. The device of claim 22 including a heater (Figure 1, 22) extending through said insulator to said chalcogenide material to heat said chalcogenide material (Specification at page 2, line 25-page 3, line 3).



At this point, no issue has been raised that would suggest that the words in the claims have any meaning other than their ordinary meanings. Nothing in this section should be taken as an indication that any claim term has a meaning other than its ordinary meaning.

# GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claim 23 is unpatentable under 35 U.S.C. § 103(a) over Ichihara in view of Horie (US 2003/0214857).

### **ARGUMENT**

A. Whether claim 23 is unpatentable under 35 U.S.C. § 103(a) over Ichihara in view of Horie (US 2003/0214857).

The rationale for the asserted combination is not clear. The embodiment relied upon in Horie is one in which a conventional semiconductor phase change memory is utilized. But this embodiment in no way suggests any reason to use a layer of chalcogenide material over a semiconductor substrate where the chalcogenide material includes a species to reduce the grain size of the chalcogenide material and a species to increase the crystallization speed. In other words, there is no teaching of any reason to make these changes in a semiconductor phase change memory, as opposed to an optical disk.

The assertion, with respect to both Mizuuchi and Ichihara, that functional limitations may be ignored is improper and is directly rebutted by the Manual of Patent Examining Procedure as recently amended. See M.P.E.P. § 2173.05(G). There, it is explained that members adapted to be positioned define structural attributes of the interrelated components, citing *In re Venezia*. In other words, the components must be so configured because the claimed increase in crystallization speed and reduction in grain size. As explained in § 2173.05(G), there is nothing wrong with defining an invention in functional terms. "A functional limitation must be evaluated and considered, just like any other limitation to claim for what it fairly conveys to a person of ordinary skill ...." Thus, it is clear that these are proper limitations and that they are not taught by Horie. As a result, there is no reason to believe that any cited reference suggests any reason to apply the claimed arrangement in a semiconductor memory which includes a semiconductor substrate and a chalcogenide material over that substrate. Moreover, the cited references do not even teach the claimed functions.

Therefore, rejection of claim 23 should be reversed.

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: October 26, 2007

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## **CLAIMS APPENDIX**

The claims on appeal are:

- 16. A semiconductor memory device comprising:
  - a semiconductor substrate; and
- a layer of chalcogenide material over said substrate, said chalcogenide material including a species to reduce the grain size of the chalcogenide material and a species to increase the crystallization speed of said chalcogenide material.
  - 17. The device of claim 16 wherein said chalcogenide material includes Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub>.
- 18. The device of claim 16 wherein the grains of the chalcogenide material are less than approximately 10 nanometers.
  - 19. The device of claim 16 wherein the species to reduce grain size includes nitrogen.
- 20. The device of claim 16 wherein the species to increase crystallization speed includes titanium.
- 22. The device of claim 16 including an insulator over said substrate and under said chalcogenide material.
- 23. The device of claim 22 including a heater extending through said insulator to said chalcogenide material to heat said chalcogenide material.
- 24. The device of claim 16 including titanium containing layer under said chalcogenide material.

25. The device of claim 24 wherein said titanium containing layer is sufficiently proximate to said chalcogenide material that titanium may diffuse into the phase change material upon heating.

#### **EVIDENCE APPENDIX**

None.

### RELATED PROCEEDINGS APPENDIX

None.